UART16750: Overview

Details

Name: uart16750
Created: 14-Jan-2009 15:23:09
Updated: 17-Feb-2009 23:56:30
SVN: Browse Statistics : View

Other project properties

Category :: Communication controller
Language :: VHDL
Development status :: Stable
WishBone Compliant :: No
Phazes :: Design done, FPGA proven

Simulation

It's possible to simulate and test the design with GHDL.
A Makefile is available for starting the simulation. The testbench creates a log file (uart_log.txt).

Description

Implements a 16550/16750 UART core.

Features

- Full synchronous design
- Pin compatible to 16550/16750
- Register compatible to 16550/16750
- Baudrate generator with clock enable
- Supports 5/6/7/8 bit characters
- None/Even/Odd parity bit generation and detection
- Supports 1/1.5/2 stop bit generation
- None or 16/64 byte FIFO mode

Project maintainers

- Witt, Sebastian

- Receiver FIFO trigger levels 1/4/8/14/16/32/56
- Control lines RTS/CTS/DTR/DSR/DCD/RI/OUT1/OUT2
- Automatic flow control with RTS/CTS
- All interrupt sources/modes

Status

- Test script creation done, should cover most functions
- Test log file available

The core was synthesized on a Altera Cyclone II, connected to x86 standard hardware and than tested with standard OS drivers from:

- Linux 2.2/2.4/2.6
- Windows 2000/XP/Vista
- *BSD
- *DOS

Todo

- Variable character time-out counter
- DMA control

Resource usage

- Altera Cyclone II
- 440 LE
- 1216 memory bits
- Frequency: 130 MHz

- Xilinx Spartan 3E
- 378 Slices
- 1 RAMB
- Frequency: 100 MHz
