

The Memory Controller Board decodes three areas that can be used for I/O. The appropriated signals on the Backplane that select the I/O-Areas are named /IOEN1, /IOEN2 and /IOEN3:

I/O-Area	Signal on Backplane	Pin at Backplane Connector	Phys. Address
1	/IOEN1	C27	2000h - 27FFh
2	/IOEN2	A27	2800h - 2FFFh
3	/IOEN3	A28	3000h - 37FFh

This is the list of currently assigned I/O-Addresses:

I/O-Area	Offset	Address Range	Device
/IOEN1  2000h -27FFh	0000h	2000h - 20FFh	reserved
	0100h	2100h - 21FFh	Interrupt Controller
	0200h	2200h - 22FFh	Multi-I/O-Unit, area 1 (Keyboard and LCD)
	0300h	2300h - 23FFh	Multi-I/O-Unit, area 2 (serial and parallel ports)
	0400h	2400h - 24FFh	Ethernet Controller
	0500h	2500h - 25FFh	reserved
	0600h	2600h - 26FFh	reserved
	0700h	2700h - 27FFh	reserved
/IOEN2  2800h -2FFFh	0000h	2800h - 28FFh	IDE-Controller / RTC, area 1
	0100h	2900h - 29FFh	IDE-Controller / RTC, area 2
	0200h	2A00h - 2AFFh	reserved
	0300h	2B00h - 2BFFh	reserved
	0400h	2C00h - 2CFFh	VGA Graphics Unit, area 1
	0500h	2D00h - 2DFFh	VGA Graphics Unit, area 2
	0600h	2E00h - 2EFFh	VGA Graphics Unit, area 3
	0700h	2F00h - 2FFFh	VGA Graphics Unit, area 4
/IOEN3  3000h -37FFh	0000h	3000h - 30FFh	unassigned
	0100h	3100h - 31FFh	unassigned
	0200h	3200h - 32FFh	unassigned
	0300h	3300h - 33FFh	unassigned
	0400h	3400h - 34FFh	unassigned
	0500h	3500h - 35FFh	unassigned
	0600h	3600h - 36FFh	unassigned
	0700h	3700h - 37FFh	unassigned

#### Notes:

- The periphery that uses I/O-Area 1 and 2 (/IOEN1 and /IOEN2) is part of the basis MyCPU-System and is most commonly supported by kernel drivers.
- The address of periphery that uses the I/O-Area 3 (/IOEN3) must be configurable through jumpers. The drivers for that periphery are not part of the kernel. The developer of that periphery is responsible for providing the driver.